REMARKS

Favorable reconsideration of this application is respectfully requested in view of the claim amendments and following remarks. Claims 1, 5, 8, 10, and 11 have been amended. Claims 4 and 9 have been canceled without prejudice or disclaimer of the subject matter contained therein. Claims 21-23 have been added. Currently, claims 1-3, 5-8, and 10-23 are pending in the present application of which claims 1, 8, 16, and 21 are independent.

No new matter has been introduced by way of the claim additions or amendments, entry thereof is therefore respectfully requested.

Claims 1-20 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Fujii et al. (U.S. Patent Number 6,140,836). The above rejections are respectfully traversed for at least the reasons set forth below.

Drawings

At the outset, the indication that the drawings have been accepted is noted with appreciation.

Title

The Official Action alleges that the title of the invention is not descriptive or is not clearly indicative of the invention to which the claims are directed. The Applicant, although in disagreement, has amended the title as set forth above without prejudice.

Abstract

The Official Action alleges that the abstract of the disclosure may be too lengthy. A replacement abstract is provided herein.

Specification

The Official Action objected to the disclosure for an alleged informality. Specifically, the Official Action alleges that the specification does not properly identify an application that is incorporated by reference. The application to which the Official Action refers is properly incorporated by reference using the attorney docket number. The specification is amended herein to include the serial number. The Examiner is respectfully requested to withdraw this object to the disclosure.

Claim Rejection Under 35 U.S.C. §102

The test for determining if a reference anticipates a claim, for purposes of a rejection under 35 U.S.C. § 102, is whether the reference discloses all the elements of the claimed combination, or the mechanical equivalents thereof functioning in substantially the same way to produce substantially the same results. As noted by the Court of Appeals for the Federal Circuit in *Lindemann Maschinenfabrick GmbH v. American Hoist and Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984), in evaluating the sufficiency of an anticipation rejection under 35 U.S.C. § 102, the Court stated:

> Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.

Therefore, if the cited reference does not disclose each and every element of the claimed invention, then the cited reference fails to anticipate the claimed invention and, thus, the claimed invention is distinguishable over the cited reference.

Claims 1-20 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Fujii et al. This rejection is respectfully traversed because the claimed invention as set forth in amended claims 1 and 8, claim 16, and the claims that depend there from are patentably distinguishable over Fujii et al.

Fujii et al. discloses a self-time pipelined data path system and an asynchronous signal control circuit. The circuits and data path system are shown in Figure 1 of Fujii et al. The asynchronous signal control circuit, labeled as such in Figure 1, includes a series of registers (reg1, reg2, reg3), a plurality of gates (nor1, nor2,...), and a series of delays (dl1, dl2). Fujii et al. also discloses combinational circuits (11A and 12A). The combinational circuits function in combination with the asynchronous signal control circuit to turn stages of the pipelined data path system on and off as data flows through the pipeline. This method is described at Column 7 Lines 29-39 of Fujii et al. For instance, if stage 1 is on, then stages 2 and 3 are off. If stage 2 is on, then stage 1 and 3 are off. If stage 3 is on, then stages 1 and 2 are off. Accordingly, only one stage is "on" at any instance of time. In particular, with reference to Figure 1 of Fujii et al., the signal SLP and SLP* dictate that as register 2 is turned on, register 1 is thereby turned off, because the signal SLP* feeds back from combinational circuit 11A to turn register 1 off. Therefore, register 1 and register 2 are not on at the same time.

According to an embodiment described in the Applicant's disclosure, a method is shown for minimizing power consumption by a circuit. A transition of an input or an output

of a pipelined circuit having a plurality of stages is detected, timed, and compared with a predetermined period of time. If a predetermined period of time expires prior to detecting a transition (the pipelined circuit is not processing data) each stage of the pipelined circuit is sequentially shut-down from a powered on state so that all stages are shut-down over a period of time. If an input transition is detected, (the pipelined circuit is processing data) each stage of the pipelined circuit is sequentially provided with power so that all stages are powered.

Claim 1

Claim 1, as amended, recites "performing a sequential shut-down procedure on each stage of said plurality of stages of said pipelined circuit in response to said predetermined period of time expiring such that each stage of the plurality of stages is shut-down." Fujii et al. fails to teach the sequential shut-down procedure such that each stage is shut-down as recited in claim 1. Fujii et al., as described above, discloses a procedure for powering stages on or off as needed, which is substantially different from sequential shut-down of all stages. Therefore, Fujii et al. fails to disclose at least this element of claim 1.

Additionally, claim 1 recites "determining whether a predetermined period of time has expired, said predetermined period of time being associated with a predetermined period of time to detect a transition of an input or an output of a pipelined circuit having a plurality of stages powered on." The Official Action alleges that Fujii et al. discloses "determining whether a predetermined period of time has expired, said predetermined period of time being associated with a predetermined period of time to detect a transition of an input or an output of a pipelined circuit" in Column 5 Lines 41-60 and Column 7 Lines 59-63. However, Fujii et al. does not teach determining whether a predetermined period of time, associated with the

detection of a transition, has expired. Fujii et al. does have a time delay device as described in those columns and lines cited by the Official Action, but the time delay is not associated with detecting a transition. Therefore, Fujii et al. also fails to disclose this element of claim 1.

In addition, claim 1 recites "...a pipelined circuit having a plurality of stages powered on." Fujii et al. fails to teach a plurality of stages powered on as recited in claim 1. Instead, Fujii et al., as described above, discloses that only one stage is on at any particular time. See Column 7 Lines 29-39. Therefore, Fujii et al. fails to disclose this element of claim 1.

Accordingly, Fujii et al. fails to teach all of the features contained in claim 1, and thus, this claim is believed to be allowable. Claims 2, 3, and 5-7 depend upon allowable claim 1 and are also allowable at least by virtue of their dependencies.

Claim 8

The Official Action alleges that claim 8 "basically are (sic) the corresponding elements that are carried out (sic) the method of operating (sic) steps in claims 1-7." However, the elements recited in claim 8 are not found in Fujii et al. For instance, Fujii et al. fails to teach the first or second transition detection circuits recited in claim 8. In addition, claim 8, as amended, recites "a stage control circuit connected to said first and said second transition detection circuits, said stage control circuit including a timer measuring a predetermined period of time and configured to sequentially control said power consumption of said pipelined circuit based on a comparison between a signal received from either said first transition detection circuit or said second transition detection circuit and the timer." Fujii et al. fails to teach the stage control circuit having a timer as recited in claim 8. Fujii et

al., as described above, discloses a delay connected to a plurality of gate devices. This arrangement is not a timer as recited in claim 8 as the delay device cannot measure time. Therefore, Fujii et al. fails to disclose at least this element of claim 8.

Furthermore, the Official Action does not show any correspondence between the circuits in Fujii et al. and the elements in claim 8. It is important for an Official Action to properly communicate the basis for a rejection so that the issues can be identified early and the Applicant can be given FAIR opportunity to reply. See MPEP §706 and §706.02(j). If the rejection to claim 8 is maintained, the rejection should not be made final as the Applicant has not been given a fair opportunity to reply.

Accordingly, Fujii et al. fails to teach all of the features contained in claim 8, and thus, this claim is believed to be allowable. Claims 10-15 depend upon allowable claim 8 and are also allowable at least by virtue of their dependencies.

Claim 16

The Official Action alleges that with regard to claim 16 "Fujii et al. teaches the claimed method of steps." However, the elements recited in claim 16 are not found in Fujii et al. For instance, Fujii et al. fails to teach the timer or an up/down sequencer as recited in claim 16. In addition, claim 16, as amended, recites "an up/down sequencer operable to perform a shut-down procedure or a turn-on procedure to control power applied to a plurality of stage circuits in said pipelined circuit...and... a timer, wherein said up/down sequencer performing said shut-down procedure in response to said timer expiring." Fujii et al. clearly fails to teach the up/down sequencer and the timer or the relation between the two as recited

in claim 16. Fujii et al., as described above, discloses a delay connected to a plurality of gate devices. However, this arrangement is not a timer as recited in claim 16 as the delay device cannot measure time. Additionally, there is no circuit in Fujii et al. resembling an up/down sequencer. Therefore, Fujii et al. fails to disclose at least these elements of claim 16.

Furthermore, the Official Action does not show any correspondence between the circuits in Fujii et al. and the elements in claim 16. It is important for an Official Action to properly communicate the basis for a rejection so that the issues can be identified early and the Applicant can be given FAIR opportunity to reply. See MPEP §706 and §706.02(j). If the rejection to claim 16 is maintained, the rejection should not be made final as the Applicant has not been given a fair opportunity to reply.

Accordingly, Fujii et al. fails to teach all of the features contained in claim 16, and thus, this claim is believed to be allowable. Claims 17-20 depend upon allowable claim 16 and are also allowable at least by virtue of their dependencies.

Accordingly, Fujii et al. fails to teach all of the features contained in claims 1, 8, and 16, and thus, these claims are believed to be allowable. Claims 2, 3, and 5-7 depend upon allowable claim 1; claims 10-15 depend upon allowable claim 8; and claims 17-20 depend upon allowable claim 16 and are also allowable at least by virtue of their dependencies. Therefore, the Examiner is respectfully requested to withdraw the rejection of claims 1-3, 5-8, and 10-20.

Newly Added Claims

Claims 21-23 have been added. Claim 21 includes elements similar to the elements in claims 1, 8, and 16 and therefore is allowable over the prior art of record for similar reasons.

Claims 22 and 23 depend upon claim 21 and are allowable at least by virtue of their dependencies. Therefore, the Examiner is respectfully requested to allow claims 21-23.

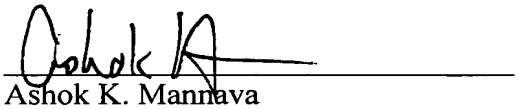
Conclusion

In light of the foregoing, withdrawal of the rejections of record and allowance of this application are earnestly solicited.

Should the Examiner believe that a telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified application, please contact the undersigned at the telephone number listed below. Please grant any required extensions of time and charge any fees due in connection with this request to deposit account no. 08-2025.

Respectfully submitted,

Joseph KU

Dated: November 10, 2004 By 

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